	Search Text
1	transparen$4 near3 latch$4 and clock adj2 (buffer driver) and local$4
2	(transparen$4 near3 latch$4 and clock adj2 (buffer driver) and local$4) and (sta timing near3 (model$4 behavior$4))
3	((transparen$4 near3 latch$4 and clock adj2 (buffer driver) and local$4) and (sta timing near3 (model$4 behavior$4))) and ((clock adj2 (buffer driver) same local$4) or lcb)
4	(((transparen$4 near3 latch$4 and clock adj2 (buffer driver) and local$4) and (sta timing near3 (model$4 behavior$4))) and ((clock adj2 (buffer driver) same local$4) or lcb)) and delay same user
5	((((transparen$4 near3 latch$4 and clock adj2 (buffer driver) and local$4) and (sta timing near3 (model$4 behavior$4))) and ((clock adj2 (buffer driver) same local$4) or lcb)) and (setup set adj up)) and (transparen$4 near3 latch$4) same allow$6
6	(((transparen$4 near3 latch$4 and clock adj2 (buffer driver) and local$4) and (sta timing near3 (model$4 behavior$4))) and ((clock adj2 (buffer driver) same local$4) or lcb)) and (setup set adj up)

	Search Text
1	allow$4 same transparent$4 same latch$4
2	(allow$4 same transparent$4 same latch$4) and 716/$.ccls.
3	allow$4 same transparen$4 same latch$4 same (timing) same (behavior model$4 static simulat$4 synthes$4)
4	allow$4 same transparen$4 same latch$4 same (timing) same (behavior model$4 static simulat$4 synthes$4) and clock same delay$4 same (launch$4 relaunch$4 re adj launch$4)
5	(mak$4 permi$5) same transparent$4 same latch$4
6	(mak$4 permi$5) same transparen$4 same latch$4
7	(mak$4 permi$5) same transparen$4 same latch$4 and clock adj (buffer driver)
8	(mak$4 permi$5) same transparen$4 same latch$4 and clock adj (buffer driver) and delay same (latch$4 buffer driver)
9	(mak$4 permi$5) same transparen$4 same latch$4 and clock adj (buffer driver) and delay same (latch$4 buffer driver) and 716/$.ccls.
10	(mak$4 permi$5) same transparen$4 same latch$4 same timing same (model$4 static anal$7 simul$4 synthes$7) and clock adj (buffer driver) and delay same (latch$4 buffer driver)
11	transparen$4 same latch$4 same timing same (model$4 static anal$7 simul$4 synthes$7) and clock adj (buffer driver) and delay same (latch$4 buffer driver)
12	transparen$4 same latch$4 same timing same (model$4 static anal$7 simul$4 synthes$7) and clock adj (buffer driver) and delay same (latch$4 buffer driver) and delay same latch$4
13	transparen$4 same latch$4 same timing same (model$4 static anal$7 simul$4 synthes$7) and clock adj (buffer driver) and delay same (latch$4 buffer driver) and delay same latch$4 and (user engineer designer) same delay